REMARKS

Claims 1-17 are pending. The Examiner's reconsideration of the rejections is respectfully requested in view of the amendments and remarks.

Applicants appreciate the courtesies extended by the Examiner during the telephone conversation of December 13, 2005, during which the time period for reply was discussed. The Examiner indicated that the time for reply is three months from the date of the Office Action.

The Specification has been objected to as being so incomprehensible as to preclude a reasonable search of the prior art by the Examiner. The Examiner suggested, as an example, that a certain paragraph be amended to point to Figure 3.

Respectfully, the paragraph cited in the example appears as part of the Summary of the Invention. References to the figures are prohibited in the Summary of the Invention. Therefore, Applicant's point the Examiner to the Detailed Description of Preferred Embodiments, which describes embodiments with reference to the various figures of the application. For example, see paragraphs [0034-0039], which clearly describes the paragraph cited in the Office Action.

Further, Tables 1, 2 and 3 have been added, which put in tabular form the examples given with respect to Figures 3, 4 and 5, respectively.

The Examiner's reconsideration of the rejection is respectfully requested.

Claims 1-4, 6, 8 and 11 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Referring to claims 1-3, the Examiner has indicated, essentially that the CPU occupancy rate is not distinctly claimed.

Using claim 1 as an example; claim 1 claims, *inter alia*,

"applying a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, and the first bus occupancy rates for the second and third master devices to a bus arbiter, in response to an activation of an interrupt signal provided to the CPU;

applying a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, and the first bus occupancy rates for the second and third master devices to the bus arbiter, in response to an inactivation of the interrupt signal."

Portions of claim 1 have been underlined for emphasis. As can be seen, a rate of the CPU changes from a first bus occupancy rate to one of a second bus occupancy rate or a third bus occupancy rate in response to an activation or deactivation of the interrupt signal, respectively.

Therefore, claim 1 is believed to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 2 and 3 include similar limitations and are believed to be allowable for at least the reasons given for claim 1.

Referring to claim 4, claim 4 claims, *inter alia*,

"a bus arbiter receiving either a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to an interrupt signal provided to the CPU, receiving the first bus occupancy rates for the second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices."

Portions of claim 4 have been underlined for emphasis. As can be seen, the bus arbiter receives either a second or a third bus occupancy rate in response to an interrupt signal. Therefore, claim 4 is believed to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 6, 8 and 11 include similar limitations to claim 4, wherein the bus arbiter receives either a second or a third bus occupancy rate in response to a signal. Thus, claims 6, 8 and 11 are believed to be allowable for at least the reasons given for claim 4.

Claim 5 depends from claim 4. Claim 7 depends from claim 6. Claims 9 and 10 depend from claim 8. Claims 12 and 13 depend from claim 11. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. For the foregoing reasons, the Examiner's reconsideration of the rejection is respectfully requested.

Claims 14-17 have been rejected under 35 U.S.C. 102(b) as being anticipated be LeBerge (USPN 6,654,833). The Examiner stated essentially that LeBerge teaches all the limitations of claims 14-17.

Claim 14 claims, "A PCI bus system comprising: a PCI bus coupled to a plurality of slots; a host device coupled to the PCI bus, the host device controlling the PCI bus system; a device storing bus occupancy rates for a plurality of cards inserted into respective slots and a variable bus occupancy rate for increasing or decreasing the bus occupancy rates; and a bus arbiter controlling a priority for use of the PCI bus in accordance with the bus occupancy rates for the cards in response to interrupt signals generated by the cards. Claim 17, claims, "A card bus system comprising: a plurality of cards coupled to a card bus; a host device coupled to the card bus, controlling the card bus system; a device storing bus occupancy rates for the cards and a variable bus occupancy rate for increasing or decreasing the bus occupancy rates; and a bus

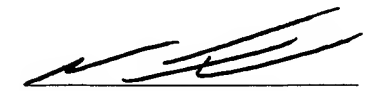
arbiter controlling a priority for use of the card bus in accordance with the bus occupancy rates for the cards in response to interrupt signals generated by the cards."

LeBerge teaches a method including permitting a first bus agent to access a bus during predetermined windows of time and preventing a second bus agent from accessing the bus outside of the windows (see Abstract). LeBerge does not teach a device storing "a variable bus occupancy rate for increasing or decreasing the bus occupancy rates" as claimed in claims 14 and 17. LeBerge teaches a register for storing a predetermined number of clock signals during which a device may use a bus (see col. 4, lines 36-59). LeBerge does not teach or suggest a register storing bus occupancy rates. The number of clock signals of LeBerge is a time-based measurement. The number of clock signals is not analogous to a variable bus occupancy rate; nowhere does LeBerge teach storing a bus occupancy rate. Therefore, LeBerge fails to teach all the limitations of claims 14 and 17.

Claims 15 and 16 depend from claim 14. The dependent claims are believed to be allowable for at least the reasons given for claim 14. The Examiner's reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including claims 1-17, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

By: 

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